CLAIMS

1. A power supply control method comprising:

coupling an input of a power supply system to receive an input voltage having a period;

coupling a load to receive the input voltage;

forming a power supply controller to generate a load current through the load when the input voltage is greater than a first voltage; and

forming the power supply controller to disable the load current when the input voltage is greater than a second voltage.

2. The method of claim 1 further including forming the power supply system to disable the load current when the input voltage is less than the first voltage.

3. The method of claim 1 wherein coupling the input of the power supply system to receive the input voltage includes coupling the input of the power supply system to receive a rectified dc voltage.

4. The method of claim 1 wherein forming the power supply controller to generate the load current through the load when the input voltage is greater than the first voltage includes forming the power supply controller to drive an output transistor of the power supply controller in a liner mode to generate an instantaneous current that averages to a desired average current over the period.

5. The method of claim 4 wherein forming the power supply controller to disable the load current when the input voltage is greater than the second voltage includes forming the power supply controller to disable the load current when a voltage drop across the output transistor is a third voltage that is representative of the second voltage.

6. The method of claim 4 wherein forming the power supply controller to drive the output transistor of the power supply controller in the liner mode to generate the instantaneous current includes forming the power supply controller to generate an averaged signal that is representative of an average value of the load current.

7. The method of claim 6 wherein forming the power supply controller to drive the output transistor of the power supply controller in the liner mode to generate the instantaneous current includes forming the power supply controller to generate a deviation signal representative of a difference between the averaged signal and a reference signal, and to generate an error signal representative of a difference between the deviation signal and the instantaneous current.

8. The method of claim 1 wherein forming the power supply controller to generate the load current through the load when the input voltage is greater than the first voltage; and forming the power supply controller to disable the load current when the input voltage is greater than the second voltage includes forming the power supply controller to generate the load current each time the input voltage is greater than the first voltage and less than the second voltage.

9. A power supply controller comprising:

an averaging circuit coupled to receive an input signal representative of a load current through a load of the power controller and form an averaged signal representative of an average value of the load current;

a first amplifier coupled to receive the averaged signal and a first reference voltage and responsively form a deviation signal representative of a difference between the averaged signal and the first reference voltage;

a second amplifier coupled to receive the deviation signal and the input signal and responsively drive an output transistor to generate the load current through the load on a current output of the power controller; and

a disable circuit coupled to responsively disable the output transistor when a voltage across the output transistor is greater than a first value.

10. The power supply controller of claim 9 wherein the averaging circuit coupled to receive the input signal representative of the load current through the load of the power controller and form the averaged signal representative of the average value of the load current includes a transconductance amplifier coupled to receive the input signal and a filter coupled to an output of the transconductance amplifier.

11. The power supply controller of claim 9 wherein the averaging circuit coupled to receive the input signal representative of the load current through the load of the power controller and form the averaged signal representative of the average value of the load current includes a sense circuit coupled to receive the load current, generate a sense current representative of the load current, generate a sense voltage from the sense current, and use the sense voltage as the input signal.

12. The power supply controller of claim 9 wherein the disable circuit coupled to responsively disable the output transistor when the voltage across the output transistor is greater than the first value includes a comparator coupled to receive the voltage across the output transistor and a reference voltage and responsively disable the output transistor.

13. The power supply controller of claim 12 wherein the comparator coupled to receive the voltage across the output transistor and the reference voltage and responsively disable the output transistor includes the comparator coupled to disable the output transistor when the first voltage is between two and fifteen volts.

14. The power supply controller of claim 9 wherein the first amplifier coupled to receive the averaged signal and a first reference voltage includes a differential amplifier.

15. A method of forming a power supply controller comprising:

coupling an output transistor to form a load current through a load that is coupled to an output of the power supply controller;

forming an averaging circuit to receive an input signal representative of the load current and responsively form an averaged signal representative of an average value of the load current;

forming the power supply controller to generate a deviation signal representative of a difference between the averaged signal and a desired constant;

forming the power supply controller to drive the output transistor responsively to a difference between the deviation signal and the input signal to generate an instantaneous value of the load current that will result in an average value of the load current over a first time period; and

forming a disable circuit coupled to responsively disable the output transistor when a voltage across the output transistor is greater than a first value.

16. The method of claim 15 wherein forming the disable circuit coupled to responsively disable the output transistor when the voltage across the output transistor is greater than the first value includes forming the disable circuit to disable the output transistor at least once during the first time period.

17. The method of claim 15 wherein forming the averaging circuit to receive the input signal representative of the load current and responsively form the averaged signal representative of the average value of the load current includes coupling a first amplifier to receive the input signal, coupling a filter to receive an output of the first amplifier, and coupling the output of the first amplifier to an input of a second amplifier.

18. The method of claim 15 wherein forming the power supply controller to generate the deviation signal representative of the difference between the averaged signal and the desired constant includes forming a deviation circuit having an amplifier coupled to receive the averaged signal and a reference signal and responsively form the deviation signal representative of the difference between the averaged signal and the reference signal.

19. The method of claim 15 wherein forming the power supply controller to drive the output transistor responsively to the difference between the deviation signal and the input signal includes forming the output transistor to sink the load current from the load wherein the load current is supplied by a rectified dc voltage applied to the load and wherein a period of the rectified dc voltage forms the first time period.

20. The method of claim 15 wherein forming the disable circuit coupled to responsively disable the output transistor when the voltage across the output transistor is greater than the first value includes forming a comparator coupled to receive the voltage across the output transistor and receive a reference voltage and responsively disable the output transistor when the voltage across the output transistor is greater than the reference voltage.